Mohammad Y. Omara

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OBJECTIVE

To obtain a challenging position in a Hi-Tech reputable company or educational establishment that makes use of my engineering and academic design skills, and adds me values at the same time.

PERSONAL INFORMATION

Date Of Birth	September 12th, 1976
Military Status	Exempted
Marital Status	Engaged

EDUCATION

Information Technology Institute, 1999-2000 ***Egyptian Cabinet***

Very Large Scale Integration (VLSI) Post-Graduate Studies. A Post-Graduate Scholarship offered by the National Egyptian **Information Technology Institute** (***iTi***) , the famous prestigious post-graduate school of the Egyptian **Information and Decision Support Center** (***IDSC***) , that is part of the **Egyptian Ministerial Cabinet**.
The scholarship is offered by the (***iTi***) in cooperation with ***Mentor Graphics International***.
Supervisor: **Dr. Hani Fekry Ragae** (Ain Shams University)
Grade: **Distinction**

(Post-Graduate courses and thesis/project description are attached in the last 2 pages of the resume. The thesis document is available upon request)

Alexandria University, 1994-1999 ***Alexandria, Egypt***

B.Sc. in Communications and Electronics
Grade: Good
Graduation Project: *Wireless Local Area Network (PHY-LAYER) Design.*
Graduation Project Grade: Distinction

CAREER HISTORY

2001 (Jan.) – **2003** (Sept.) Embedded Systems Designer at ***Ellipsis Digital Systems Inc.***, an international semiconductor technology company that develops integrated circuits and software solutions for broadband communication systems.
Working under the management of **Dr. Khalid Ismail**, an IEEE fellow, **MIT** (Massachusetts Institute of Technology) PhD Holder and an Associate Professor at many reputable international universities. **Dr. Khalid Ismail** is the founder of the **SiGe** Technology and a holder of many US registered Patents in Microelectronic Devices.

2000(July.) – **2001**(Jan.) VLSI Teaching Assistant in the (***iTi***).

1999(Sept.) – **2000**(Jul.) Trainee in ***Mentor Graphics*** International (***iTi*** period).

1998 (Jun. – Sept.) Summer jobs in **USA**: Salesman in a warehouse.

QUALIFICATIONS

Programming VHDL, C/C++, Java, Sun Microsystems standard JVM and Intel's X86 and 8051 assemblies. Familiar with Verilog, TCL and Visual Basic.

Operating Systems Windows (all), UNIX (Solaris), Linux (Red Hat).

EDA Tools ***Mentor Graphics*** IC design flow (Windows-based and UNIX-based tools) , ***Xilinix*** Alliance and ISE , ***Altera*** MAX Plus , ***Cadence*** Orcad and PSpice , ***Aldec*** ActiveHDL , ***UC Berkeley*** Ptolemy.

Software MATLAB, Visual Studio, Visual Café, MS Office, Prism Editor (for HDL), Macromedia (Flash, Fireworks), Adobe PhotoShop ME.

EXPERIENCE

JAVA Java for embedded systems, Java Ahead-Of-Time compilers (like GCC-GCJ), also various virtual machines for embedded systems' applications.

Communication Systems	IEEE 802.11x standards for Wireless LAN, Bluetooth, DSP blocks (FFT/IFFT, Convolutional Encoder, Interleaver / De- interleaver, Scrambler / De- scrambler, Viterbi Decoder, AGC, De-Map, De-Proc, Equalizers) and RF Front-ends/Interfaces.
Microprocessor and Embedded Systems	Good knowledge of Microprocessor Architecture and Design, Multiprocessor systems (scheduling and synchronization) and the use of heterogeneous environment simulators like Ptolemy for modeling, simulation and design of concurrent, real-time, embedded systems. Familiar with bus systems and Real Time Operating Systems (RTOS).
VHDL	Skilled in modeling systems with VHDL, VHDL coding for synthesis, Generic design, Package design, VHDL Verification and exhaustive test bench design, and dealing with VHDL/Verilog Mixed Environment.
ASSEMBLY	Fair knowledge of the Assembly Languages of most of the market widely spreading processor families like: Intel families (like 8051 microcontroller), Motorola families, PIC microcontroller, OpenRISC … etc. Writing assembly programs to run the IEEE 802.11a based wireless LAN multiprocessor Embedded system

PROJECTS

1- **Extended ISA Design** of the specific purpose digital signal processors used in implementing the IEEE 802.11a based wireless LAN multiprocessor embedded system. The methodology used in designing these MISPs (Matched Instruction Set Processors) is being filed as Patent(s) in the Governmental US Patents Organization forming a new methodology for designing Digital Communication Systems.

2- **FFT/IFFT MISP**:
The whole design and integration process was completed during the project period that I have stayed in Ellipsis San Diego Headquarters. The FFT/IFFT MISP was the first processor to be designed by Ellipsis.
The project was under the supervision of **Dr. Vason Sirini.**
(Dr. Vason Sirini is a Berkeley Professor and a Patent holder in the field of microprocessor Design).
The verification process was completed in Ellipsis Cairo Engineering Center.

3- **Viterbi Decoder MISP**: A Viterbi Decoder specific processor for Error Detection and Correction in the IEEE 802.11a WLAN receiver. The most critical aspect of this component was to achieve the speed requirements of the IEEE 802.11a standard specifications. The processor was completely verified with various exhaustive Java/assembly programs.

4- **Sample Buffer MISP**: A specific purpose processor located at the beginning of the Transceiver chain of IEEE 802.11a WLAN embedded system. The role of the Sample Buffer is to organize the data samples moving between the RF Interface and the base-band chain. The processor was completely verified with various exhaustive Java/assembly programs.

5- **Automatic Gain Control (AGC) :** The processor is implemented in two different architectures:

1- Turbo mode architecture: It implements an extended ALU that contains some auxiliary instructions to parallelize the processing of the AGC (MISP Architecture).
2- Normal mode architecture: It excluded the extended ALU to force the AGC to use only basic arithmetic/logic and program flow instructions to calculate and process the gain within time-line borders.

6- **Modem Radio Controller (MRC) Model:** A complete model has been designed to emulate the existence of the PHY layer Controller of the IEEE 802.11a based wireless LAN system while verifying other individual PHY layer components (like FFT/IFFT, AGC..etc.).

7- **Interface Components:** Two interface components were designed to interface both Data and Control Buses. The development of these two components resulted in standardizing them to be the standard Data/Control Bus Interface of any stand-alone IP in the system.

ACTIVITIES

1- One of the registered designers of the ***OpenCores.org*** International Organization for Open Source Hardware Designs.
2- One of the founders and designers of the Arabic organization (Teq-3al) for Open Source Hardware Designs (currently working on its pilot project, an open source PDA).

LANGUAGES

English (Fluent: spoken, written, read). TOEFL score: 590.
Arabic (Mother tongue)

REFERENCES

Available upon request

The Egyptian Cabinet
The Information and Decision Support Center (IDSC)
The Information Technology Institute (iTi)

Courses included in the iTi scholarship:

General IT courses:

1. Primer on S/W Development.
2. Presentations skills.
3. Computer Architecture/Operating System.
4. Modern database Systems & SQL.
5. Computer Networking.
6. S/W Engineering.
7. C, C++.
8. Visual Basic Programming Language.
9. Management Fundamentals.
10. S/W project Management.
11. Problem Solving Techniques.
12. Developing Communication Skills.
13. Technical Writing.
14. Accounting and Finance.
15. Marketing.
16. Introduction to **UNIX** Operating System.
17. **Win NT 4.0** Microsoft Operating System:
    - Win NT 4.0 workstation
    - Win NT 4.0 server
    - Win NT core technology and administration .

VLSI Platform courses:

1. Electronic Circuit Design.
2. Logic Design.
3. Computer Organization.
4. VHDL for Synthesis.
5. VLSI Technology.
6. VLSI Device Modeling.
7. VLSI Circuit Design.
8. Synthesis and Verification of VLSI Systems
9. Embedded System Design.
10. HW/SW Co-Design.
11. Design for testability (DFT).
12. FPGA/ASIC Design.

EDA Tools:

Mentor Graphics tools:

1. FPGA Advantage (Packaged power new version) which includes:
   i. Renoir: Design entry tool.
   ii. ModelSim: Digital Simulation tool.
   iii. Leonardo Spectrum: Synthesis tool.
2. IC_station: for integrated circuits layout design.
3. QuickSim: for digital circuits' simulation.
4. Design Architect: schematics design tool
5. Seemless CVE (Co-Verification Environment): tool for S/W_H/W co verification.
6. AccueSim: for analog circuits' simulation.

Altera tools: *MAX+PLUS II*

Xilinix tools: *ALLIANCE* tool for FPGA

Thesis and Project:

Viterbi Decoder

The project aimed to produce a digital Viterbi Decoder chip (integrated circuit), that is used in communication systems just like digital satellite receivers (QPSK digital satellite receiver system design is studied during the project period). The Viterbi Decoder is based on the well-known Viterbi Algorithm for error detection and correction. The microelectronic design targets both ***FPGA*** and ***ASIC***. The project is designed and simulated on Mentor Graphics' tools using AMS 0.8-micron CYB process library.

RF Mixer

Variable gain RF mixer used in wireless communication systems' RF front ends. The project is on the simulation level.

Ellipsis
Digital Systems
...Software for Reconfigurable Hardware

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www.ellipsisdigital.com

Reference Letter

To Whom It May Concern: 20 October 2003

Mr. Mohammad Youssef Omara was employed as a Senior Hardware Engineer at the Ellipsis Cairo Engineering Center during the period from January 2001 to September 2003. Headquartered in Carlsbad, California, USA, Ellipsis Digital Systems, Inc., was developing a System On a Chip (SoC) for Wireless Local Area Network communication systems based on the IEEE 802.11a/b standard.

Mr. Omara's specific responsibilities included:

- Hardware design of VHDL models of Matched Instruction Set processors (MISP) using Mentor Graphics design tools
- Designing the Instruction Set Architecture of the processors
- Writing assembly code for the processors
- Design and Development of communication blocks using Java

Mr. Omara is a proactive employee. He takes ownership of his assigned tasks and pursues them till they are complete, with a high focus on quality and specified requirements.

Below are some of the professional skills that Mohammed has demonstrated:

- Works smoothly with teams
- Communicates effectively
- Fast learner

Ellipsis Management appreciates Mr. Omara's contribution to the company and recommends him highly for a comparable job.

Sincerely,

Dr. Hussein S. El-Ghoroury
President & CEO
Ellipsis Digital Systems, Inc.