APPENDIX A

This appendix includes the design testbensh for HDL simulation on ModelSim, and the force files used in QuickSim.

Here is a testbench for the entire system: encoder, receiver front end, and decoder:

```verilog
/**************************************************************/
/* Module viterbi_test_CDD                                  */
/**************************************************************/
/* This is the top-level module, viterbi_test_CDD that models
the communications link. It contains three modules:
viterbi_encode, viterbi_distances, and viterbi. There is no
analog and no noise in this version. The 2-bit message, X, is
encoded to a 3-bit signal, Y. In this module the message X is
generated using a simple counter. The digital 3-bit signal Y is
transmitted, received with noise as an analog signal (not
modeled here), and converted to a set of eight 3-bit distance
measures, in0, ..., in7. The distance measures form the input
to the Viterbi decoder that reconstructs the transmitted signal
Y, with an error signal if the measures are inconsistent. CDD =
counter input, digital transmission, digital reception */
module viterbi_test_CDD;
wire Error; // decoder out
wire [2:0] Y, Out; // encoder out, decoder out
reg [1:0] X; // encoder inputs
reg Clk, Res; // clock and reset
wire [2:0] in0,in1,in2,in3,in4,in5,in6,in7;
always #500 $display("t Clk X Y Out Error");
initial $monitor("%4g",$time,,Clk,,,,X,,Y,,Out,,,,Error);
initial $dumpvars; initial #3000 $finish;
always #50 Clk = ~Clk; initial begin Clk = 0;
/**********************************************************/
```

Force files of QuickSim:

```
force reset 0 0
force reset 1 70
```

```
force in0 0 10
force in0 4 50
force in0 6 150
force in0 7 250
force in0 1 350
force in0 0 450
force in0 6 550
force in0 7 650
force in0 1 750
force in0 0 850
force in0 6 950
force in0 7 1050
force in0 1 1150
force in0 0 1250
force in0 6 1350
force in0 7 1450
force in0 1 1550
force in0 0 1650
force in0 6 1750
```

```
force in1 1 10
force in1 1 50
force in1 7 150
force in1 6 250
force in1 0 350
force in1 1 450
force in1 7 550
force in1 6 650
force in1 0 750
force in1 1 850
force in1 7 950
force in1 6 1050
force in1 0 1150
force in1 1 1250
force in1 7 1350
force in1 6 1450
force in1 0 1550
force in1 1 1650
force in1 7 1750
```

```
force in2 4 10
force in2 0 50
force in2 6 150
force in2 4 250
force in2 1 350
force in2 4 450
force in2 6 550
force in2 4 650
force in2 1 750
force in2 4 850
force in2 6 950
force in2 4 1050
force in2 1 1150
force in2 4 1250
force in2 6 1350
force in2 4 1450
force in2 1 1550
force in2 4 1650
force in2 6 1750




force in3 6 10
force in3 1 50
force in3 4 150
force in3 1 250
force in3 4 350
force in3 6 450
force in3 4 550
force in3 1 650
force in3 4 750
force in3 6 850
force in3 4 950
force in3 1 1050
force in3 4 1150
force in3 6 1250
force in3 4 1350
force in3 1 1450
force in3 4 1550
force in3 6 1650
force in3 4 1750




force in4 7 10
force in4 4 50
force in4 1 150
force in4 0 250
force in4 6 350
force in4 7 450
force in4 1 550
force in4 0 650
force in4 6 750
force in4 7 850
force in4 1 950
force in4 0 1050
force in4 6 1150
force in4 7 1250
```

```
force in4 1 1350
force in4 0 1450
force in4 6 1550
force in4 7 1650
force in4 1 1750




force in5 6 10
force in5 6 50
force in5 0 150
force in5 1 250
force in5 7 350
force in5 6 450
force in5 0 550
force in5 1 650
force in5 7 750
force in5 6 850
force in5 0 950
force in5 1 1050
force in5 7 1150
force in5 6 1250
force in5 0 1350
force in5 1 1450
force in5 7 1550
force in5 6 1650
force in5 0 1750




force in6 4 10
force in6 7 50
force in6 1 150
force in6 4 250
force in6 6 350
force in6 4 450
force in6 1 550
force in6 4 650
force in6 6 750
force in6 4 850
force in6 1 950
force in6 4 1050
force in6 6 1150
force in6 4 1250
force in6 1 1350
force in6 4 1450
force in6 6 1550
force in6 4 1650
force in6 1 1750




force in7 1 10
force in7 4 50
force in7 1 150
force in7 4 250
```

```
force in7 6 350
force in7 4 450
force in7 1 550
force in7 4 650
force in7 6 750
force in7 4 850
force in7 1 950
force in7 4 1050
force in7 6 1150
force in7 4 1250
force in7 1 1350
force in7 4 1450
force in7 6 1550
force in7 4 1650
force in7 1 1750
```

APPENDIX B

DICTIONARY

Analog-to-digital converter or conversion. (A/D or ADC) – The process of sampling an analog waveform and describing it in terms of binary digits.

Automatic gain control (AGC) – Receiver function that generates constant power output under varying power input.

Application-specific integrated circuit (ASIC) – Custom IC developed for a targeted application.

Additive white Gaussian noise (AWGN) – The common wideband channel thermal noise impairment, on which signal-to-noise ratio (SNR) is typically based.

Bit error rate or bit error ratio (BER) – A figure of merit for a digital communication link. It is the fraction of bits received in error divided by the total number of bits transported.

Binary phase shift keying (BPSK) – A digital modulation format where 1 and 0 are represented by phase shifts of 0º and 180º of the carrier.

Energy-per-bit to noise density ratio (Eb/No) – A common SNR-like figure of merit for digital communication systems, particularly those obeying Nyquist criteria. Also understood as SNR-per-bit, relates to BER for a given modulation type.

Energy-per-symbol to noise density ratio (Es/No) – A common SNR-like figure of merit for digital communication systems. Equivalent to SNR for systems obeying Nyquist criteria, it relates to BER for a given modulation type, and relates to Eb/No through number of bits per symbol.

Forward Error Correction (FEC) – Technique by which a data stream is modified to create added channel robustness, improving error rate performance .

Institute of Electrical and Electronic Engineers (IEEE) – The world famous organization.

Intermediate frequency (IF) – The carrier center frequency that often follows a frequency conversion stage operating on an RF input. Chosen for ease of subsequent processing, functionality, and standardization.

Intersymbol interference. (ISI) – Digital communication system impairment where adjacent symbols in a sequence are distorted by frequency response non-idealities, creating dispersion that interferes in the time domain with neighboring symbols.

Low noise amplifier (LNA) – RF gain device designed specifically for very low imposition of additional noise power. Used to amplify very low signals without contributing significant SNR degradation.

Local oscillator (LO) – Refers to the frequency conversion CW source used in the RF mixing process.

M-ary phase shift keying (MPSK) – Digital communication system that uses one of M phases to represent $\log_2$ (M) bits, where each symbol point in the constellation rests along the circumference of a circle. QPSK is 4-PSK.

Phase-locked loop (PLL) – Feedback control loop that provides frequency and phase synchronization of one oscillator to another reference. The range of PLL application is so vast as to make further generalization difficult, but within this column's context, PLLs are integral parts of receiver systems requiring clock and carrier recovery, frequency generation and synthesis, and other types of data synchronization.

Phase modulation (PM) – Encoding information onto a carrier waveform by varying the phase of the carrier. Mathematically related and similar to the FM waveform structure because of the relationship between frequency and phase. Generally describes analog modulation.

Radio frequency (RF) – Region of spectrum or discipline of electrical design associated with high analog frequencies that require design considerations qualitatively different from traditional analog circuit design.

Surface acoustic wave (SAW) – Filter or oscillator technology characterized by its reliance on acoustic energy and electrical/ acoustic transducers used to take advantage of impressive bandpass filter shape factors that are difficult to achieve with more traditional filter technologies.

Symbol Error Rate (SER) – Similar to the BER concept, but instead refers to the likelihood of mistake detection on the digital modulation symbols themselves, which may encode multiple bits per symbol.

Signal-to-noise ratio (SNR) – Fractional relationship between the power of the desired signal to the power of the noise signal. Typically refers to the additive thermal noise impairment.

Voltage-controlled oscillator (VCO) – Frequency-generation component whose output frequency can be varied by changing the voltage to a control port on the device.

Very large scale integration (VLSI) – Extremely high density digital circuitry technology that is implemented on a single IC.