

Error Detection and Correction in QPSK

Digital Satellite Receiver

Graduation Project

Submitted in partial fulfillment for the requirement of VLSI Diploma
from Information Technology Institute

Submitted by:

Mohammad Youssef Omara

B.Sc. of Electrical Engineering

(Electronics and Communications Engineering)

Alexandria University, 1999.

Supervised by:

Prof. Dr. Hani Fikry Ragaie

Prof. Dr. Nabil El_Nady

Cairo – 2000

STATEMENT

This dissertation is submitted to the Egyptian **Information Technology Institute** for the degree of postgraduate Diploma in Very Large Scale Integration (VLSI).

The work included in this project was carried out by the author at the **Information Technology Institute**, under the supervision of **Mentor Graphics Egypt**.

Date : 13/7/2000

Signature :

Name : Mohammad Youssef Omara

ACKNOWLEDGEMENTS

I would like to take this opportunity to express my gratitude to many individuals who have given me a lot of support and help.

First of all, I am indebted to my supervisor, Prof. Dr. Hani Fikry, for his valuable guidance and encouragement throughout the entire research. Prof. Dr. Fikry has created an indispensable environment to conduct and enjoy my research work.

I would also like to thank Prof. Dr. Hani Fikry for his invaluable comments and keen remarks. Special thanks go to Prof. Dr. Nabil El_Nady and Prof. Dr. Nabil Sayeed for their extreme care and successful leadership. I am also grateful to Engineer Ahmad Abu El_Seoud from **Mentor Graphics Egypt** and Engineer Sherif Taher from **Ain Shams University** for their support in **Mentor Graphics** tools.

I wish to thank **Mentor Graphics Egypt** for supporting this project by their tools and technical support. Without the facilities provided by **Mentor Graphics**, this project work wouldn't have been successfully completed in this quality of form.

To the best man I have ever met in my life

Bodies pass away

But souls do stay

You are always in my heart father

ABSTRACT

Error detection and correction system used in satellite links, magnetic recording, cell phones, compact disc players, wireline modems, terrestrial microwave links, and virtually anywhere that errors can be introduced by an imperfect channel is presented using the known Viterbi algorithm for maximum likelihood decoding. The proposed architecture is in a VLSI (or simply in an IC) form, which can be easily implemented on a microelectronics chip as a stand alone IC or can even be included in a higher design as an intellectual property (IP). This design used AMS CYB 0.8-micron library and tools used are Mentor Graphics'. It's believed that the Viterbi algorithm for error detection and correction is the best algorithm for maximum likelihood decoding. The decoder is fully digital which means that it can be either implemented on an FPGA or ASIC.

Table of contents

List of Figures	i
List of Tables	iii
Chapter1: Channel Coding and Viterbi Algorithm	1
1.1 CONVOLUTIONAL ENCODING.....	2
1.2 CONVOLUTIONAL ENCODER PRESENTATION	4
1.2.1 Connection Representation	5
1.2.2 Impulse Response of the Encoder	6
1.2.2.1 Polynomial Presentation	9
1.2.3 State Representation and the state diagram	10
1.2.4 The Tree Diagram	11
1.2.5 The Trillis Diagram	13
1.3 FORMATION OF THE CONVOLUTIONAL DECODING PROBLEM	15
1.3.1 Maximum Likelihood Decoding.....	15
1.3.2 Channel Models: Hard versus Soft Decisions.....	17
1.3.2.1 Binary Symmetric Channel.....	20
1.3.2.2 Gaussian Channel.....	22
1.3.3 The Viterbi Convolutional Decoding Algorithm.....	23
1.3.4 Path Memory and Synchronization.....	23
Chapter2: ASIC Design Flow	25
2.1 INTRODUCTION TO ASICs.....	25
2.2 Design Flow.....	27
2.3 ASIC Cell Libraries.....	28
2.4 Viterbi Decoder Project Design.....	29

2.4.1	Viterbi Encoder.....	29
2.4.2	The Received Signal.....	33
2.4.3	Decoder Model.....	36
2.4.4	Testing The System.....	46
2.5	Simulation Phase.....	48
2.6	Synthesis of the Viterbi Decoder.....	48
2.6.1	ASIC I/O.....	48
2.6.2	The Top-Level Model.....	49
2.7	Layout Phase.....	52
2.8	Design Rule Check.....	54
2.9	Cell compaction.....	55
2.10	Back Annotation.....	56
2.11	Layout versus schematics (LVS)	56

List of Figures

Figure 1.1	Encode/decode and modulator/demodulator part a typical Communication link.....	2
Figure 1.2	Convolutional encoder with constraint length K and rate k/n	3
Figure 1.3	A simple rate $\frac{1}{2}$ convolutional code encoder.....	5
Figure 1.4	Convolutional encoding a message sequence with a rate $\frac{1}{2}$, $K = 3$ encoder.....	8
Figure 1.5	Encoder state diagram (rate $\frac{1}{2}$, $K = 3$)	11
Figure 1.6	Tree representation of encoder (rate $\frac{1}{2}$, $K = 3$).....	12
Figure 1.7	Encoder trellis diagram (rate $\frac{1}{2}$, $K = 3$).....	14
Figure 1.8	Hard and soft decoding decisions.....	18
Figure 1.9	Formulation of the convolutional Decoding Problem.....	21
Figure 2.1	An integrated circuit (IC). (a) A pin-grid array (PGA) package. (b) The silicon die or chip is under the package lid.....	26
Figure 2.2	ASIC design flow.....	27
Figure 2.3	A state diagram for a rate $\frac{2}{3}$ Viterbi encoder.....	30
Figure 2.4	The signal constellation for an 8 PSK (phase-shift keyed) code.....	32
Figure 2.5	Flow chart describing the behavior of the D flip flop.....	37
Figure 2.6	Block diagram of the subset_decode module	38
Figure 2.7	Block diagram of the metric module	38
Figure 2.8	Block diagram of the compute_metric module	39

Figure 2.9	Block diagram of the compare_select module.....	40
Figure 2.10	Block diagram of the path module.....	41
Figure 2.11	Block diagram of the path_memory module.....	42
Figure 2.12	Block diagram of the pathin module.....	43
Figure 2.13	Block diagram of the output_decision module.....	44
Figure 2.14	Block diagram of the reduce module.....	45
Figure 2.15	Simulation results using the design testbench.....	47
Figure 2.16	Synthesis Viterbi decoder (top level).....	48
Figure 2.17	Component1 (Viterbi).....	49
Figure 2.18	Component2(Subset_decode).....	49
Figure 2.19	Component3(Path).....	50
Figure 2.20	Component4(Metric).....	50
Figure 2.21	Top level design after power pads insertion manually.....	51
Figure 2.22	Viterbi decoder layout.....	52
Figure 2.23	Back Annotation results on QuickSim	55

List of Tables

Table 2.1	State table for the rate 2/3 Viterbi encoder.....	31
Table 2.2	A sequence of transmitted signals for the rate 2/3 Viterbi encoder....	32
Table 2.3	Receiver distance measures for an example transmission sequence...	34
Table 2.4	Receiver distance measures for an example transmission sequence...	35
Table 2.5	Output from the Viterbi testbench.....	46